

an array processor for performing arithmetic calculations, the array processor coupled to the interface circuit to receive information therefrom and connected to the embedded processor via an internal bus; and

wherein the array processor comprises:

a first multiply/accumulator (MAC) unit coupled to a first local memory, the first local memory comprising a first plurality of operands;

a second MAC unit coupled to a second local memory, the second local memory comprising a second plurality of operands; and

a first shared operand unit coupled to the first MAC unit and the second MAC unit for providing a first shared operand to the first MAC unit for computing a first result in association with the first plurality of operands and to the second MAC unit for computing a second result in association with the second plurality of operands; and

wherein the first result and the second result are computed independently of each other; and

wherein the array processor further comprises:

a second shared operand unit coupled to a third MAC unit and a fourth MAC unit for providing a second shared operand to the third MAC unit and the fourth MAC unit.

3. The integrated circuit according to claim 1 wherein said interface circuit includes a wire bundle for providing wide access data transfers between the interface and said array processor, and wherein said wire bundle comprises at least 256 wires.

10. An integrated circuit using a memory, said integrated circuit comprising: an interface circuit configured to control access to said memory, said interface circuit coupled to said memory;

a embedded processor configured to control said integrated circuit, said embedded processor receiving information from said interface circuit; and

an array processor for performing mathematical calculations on data received from said interface circuit and connected to said embedded processor via an internal bus, said array processor comprising:

a plurality of multiplier/accumulator circuits; and

10 a plurality of shared operand circuits coupled to said plurality of
11 multiplier/accumulator circuits for providing a shared operand to at least two of said plurality of
12 multiplier/accumulator circuits.

1 11. The integrated circuit according to claim 10 wherein said interface circuit
2 includes a wire bundle for providing wide access data transfers between the interface and said array
3 processor, and wherein said wire bundle comprises at least 256 wires.

2 12. The integrated circuit according to claim 10 wherein separate instruction and
data streams are maintained for said array processor.

1 13. The integrated circuit according to claim 10 wherein separate instruction and
2 data streams are maintained for said embedded processor.

1 14. The integrated circuit according to claim 10 wherein said interface circuit is a
2 Master Memory Interface Controller (MMIC) circuit.

1 15. The integrated circuit according to claim 10 wherein a multiplier/accumulator
2 circuit of said plurality of multiplier/accumulator circuits comprises a computational unit that
3 multiplies a first operand by a second operand to obtain a result and then adds or subtracts from said
4 result a third operand, wherein said operands are either scalars or vectors.

1 16. The integrated circuit according to claim 10 further comprising
2 a global external bus unit for providing an interface between said integrated circuit
3 and said external environment, said global external bus unit coupled to said embedded
4 microprocessor by a system bus and by a separate dedicated bus.

1 17. The integrated circuit according to claim 10 wherein said array processor
2 performs a plurality of vector operations selected from a group consisting of addition of a plurality
3 of vectors and multiplying a vector by a scalar.

1 18. The integrated circuit according to claim 10 wherein said array processor is
2 configured to share a plurality of scalar elements among a plurality of vector components of a
3 vector, wherein a first scalar element of said plurality of scalar elements mathematically operating
4 on a first vector component of said plurality of vector components and a second scalar element of

5 said plurality of scalar elements mathematically operating on a second vector component of said
6 plurality of vector components are calculated in parallel.

1 19. The integrated circuit according to claim 10 wherein said array processor uses
2 a simplified IEEE floating point notation which excludes said IEEE floating point exceptions,
3 comprising underflow, overflow, divide by zero, inexact, and invalid.

1 20. The array processor of claim 10 further comprising:
2 a front end unit for determining a fixed point result by performing a fixed point
3 addition or subtraction on a plurality of operands;
4 a floating point conversion unit for converting said fixed point result to a first floating
5 point result; and
6 a multiplier and accumulator unit for determining a second floating point result by
7 performing a floating point multiplication and then accumulation using at least said first floating
8 point result.

1 21. An integrated circuit for image frame rendering applications, said integrated
2 circuit during operation operating with memory, said integrated circuit comprising:
3 an interface circuit configured to control access to said memory, said interface circuit
4 coupled to said memory;
5 a processor embedded in said integrated circuit, said processor receiving information
6 from said interface circuit; and
7 an array processor coupled to said interface circuit and to said processor via an
8 internal bus;
9 wherein the array processor is configured to:
10 determine a fixed point result by performing a fixed point addition or subtraction on a
11 plurality of fixed point operands;
12 convert the fixed point result to a first floating point result; and
13 determine a second floating point result by performing a floating point multiplication
14 and then accumulation using the first floating point result and at least one floating point operand.

1 22. The integrated circuit according to claim 21 wherein said array processor
2 comprises: